AMENDMENTS TO THE CLAIMS:

Claims 1 - 11. (Canceled)

Claim 12. (Currently amended) A method of manufacturing a MOS transistor of LDD structure, comprising the steps of:

forming a nitride insulating film on a surface of silicon substrate;

forming a gate electrode in a predetermined pattern on a surface of said nitride insulating film;

performing wet etching of said nitride insulating film with said gate electrode used as a mask;

forming an oxide insulating film thicker than said nitride insulating film under each of both end portions of said gate electrode where said nitride insulating film is removed;

forming lightly doped source/drain area in surface portions of said silicon substrate with said gate electrode used as a mask;

forming sidewalls on said lightly doped source/drain areas; and

forming deeply doped source/drain areas in surface portions of said silicon substrate with said sidewalls used as masks.

Claim 13. (Currently amended) The method of manufacturing a MOS transistor of LDD structure according to claim 12, wherein said step of performing wet etching removes a portion of said nitride insulating film not masked by said gate electrode and removes portions of said nitride insulating film under both end portions of said gate electrode.

Claim 14. (Currently amended) The method of manufacturing a MOS transistor of LDD structure according to claim 12, wherein said nitride insulating film is comprises a silicon oxynitride film, and said oxide insulating film is comprises a silicon thermal oxidation film formed through thermal oxidation.

Claim 15. (Currently amended) The method of manufacturing a MOS transistor of LDD structure according to claim 13, wherein said nitride insulating film is comprises a silicon oxynitride film, and said oxide insulating film is comprises a silicon thermal oxidation film formed through thermal oxidation.

Claim 16. (Currently amended) A method of manufacturing a MOS transistor of LDD structure, comprising the steps of:

forming a nitride insulating film on a surface of silicon substrate;

forming a gate electrode in a predetermined pattern on a surface of said nitride insulating film;

performing wet etching of said nitride insulating film with said gate electrode used as a mask;

forming lightly doped source/drain areas in surface portions of said silicon substrate with said gate electrode used as a mask;

forming sidewalls on said source/drain areas an oxide insulating film integrally with said sidewalls under each of both end portions of said gate electrode where said nitride insulating film is removed by a CVD (Chemical Vapor Deposition) method; and

Docket No. NEC01P065-SYa 7
In re <u>divisional</u> patent application of 09/824,672 filed on April 4, 2001

forming deeply doped source/drain areas in surface portions of said silicon substrate with said sidewalls used as masks.

Claim 17. (Currently amended) The method of manufacturing a MOS transistor of LDD structure according to claim 16, wherein said step of performing wet etching removes a portion of said nitride insulating film not masked by said gate electrode and removes portions of said nitride insulating film under both end portions of said gate electrode.

Claim 18. (Currently amended) The method of manufacturing a MOS transistor of LDD structure according to claim 16, wherein said nitride insulating film is comprises a silicon oxynitride film, and said oxide insulating film is comprises a silicon oxide film.

Claim 19. (Currently amended) The method of manufacturing a MOS transistor of LDD structure according to claim 17, wherein said nitride insulating film is comprises a silicon oxynitride film, and said oxide insulating film is comprises a silicon oxide film.